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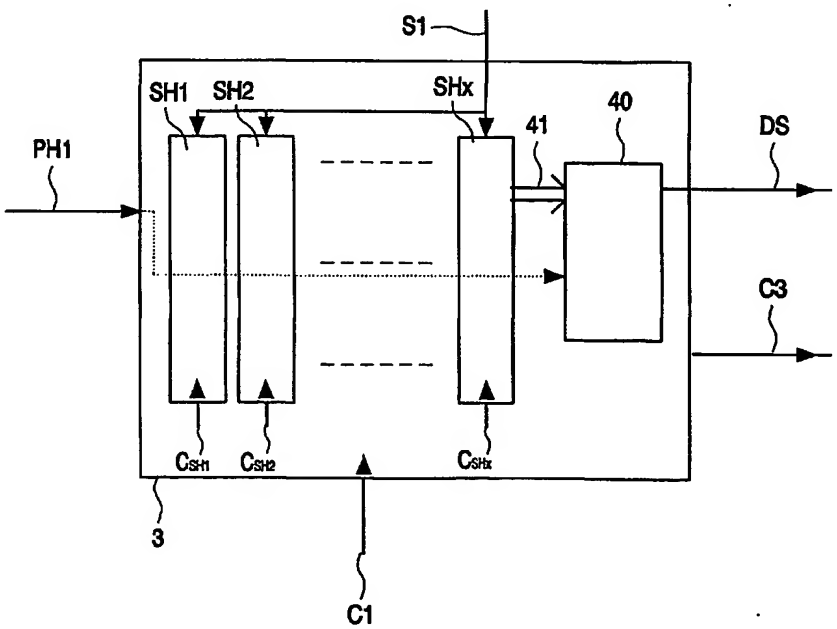
(54) Title: BIT-DETECTION ARRANGEMENT AND APPARATUS FOR REPRODUCING INFORMATION



(57) Abstract: Disclosed is a bit-detection arrangement able to convert an analog signal (AS) having an amplitude into a digital signal (DS) representing a bit sequence from which the analog signal (AS) is derived. The bit-detection arrangement has a phase detector which detect the phase difference between a quantized analog signal and a clock signal C_2. The phase difference is sampled by an AD converter. The AD converter can sample at a relatively slow rate as the phase difference is a low frequency signal. The sampled phase difference is fed to a digital PLL which outputs a phase signal PHI. The phase signal and the quantized analog signal are used to recreate the digital signal (DS). The current invention is characterized in that the bit decision unit further comprises - at least one additional sample and hold unit SH_2 able to sample the output signal S_1, using a clock signal C_{SH2} and wherein the frequency of the clock signal C_{SH2} is equal to the frequency of clock signal C_{SH1} and the phase of clock signal C_{SH2} is substantially different from the phase of clock signal C_{SH1}, and an output unit for outputting samples of either the sample and hold units SH_1 or SH_2, wherein the samples of the sample and hold unit SH_1 are outputted when the phase signal PH_1 indicates that the phase difference ΔP_1 is in a first region and the samples of the additional sample and hold unit SH_2 are outputted when the phase signal PH_1 indicates that the phase difference ΔP_1 is in a second region. This has the advantage that the change of bit errors occurring in the presence of phase jitter is reduced.

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